23 are electrically connected with the gate pad electrode 34 and the data pad electrode 36 via a gate pad contact hole 44 and a data pad contact hole 42, respectively. The gate pad electrode 34 and the data pad electrode 36 are electrically connected with external driving circuits (not shown) that drive the TFT "S" and the pixel electrode 14.

On page 6, paragraph beginning on line 15:

Next, as shown in Figure 3D, an insulating layer is deposited and patterned using a fourth mask to form a passivation layer 56, which serves to protect the active layer 55. The passivation layer 56 is either an inorganic material such as silicon oxide (SiO_2), or an organic material such as benzocyclobutene (BCB). Those materials have high light-transmittance, good humidity resistance, and good reliability, all of which are required. In addition, a data pad contact hole 42, a drain contact hole 32, and a storage contact hole 42 are formed through the passivation layer 56 to expose portions of the second storage electrode 58, the drain electrode 30, and the data pad 23. The drain contact hole 32 and the storage contact hole 40 respectively serve to electrically connect the drain electrode 30 and second storage electrode 58 to a pixel electrode 14 (see Figure 2 and Figure 3E). Further, the data pad contact hole 42 serves to electrically connect the data line 24 with a data pad electrode 36 (also see Figure 2 and Figure 3E).

On page 7, paragraph beginning on line 22:

Figure 4 is a cross-sectional view taken along a line "IV-IV" of Figure 2. As shown, a gate pad 21 electrically contacts a gate pad electrode 34. First, a gate pad 21 is formed on the substrate 1. Then, a gate insulating layer 50, an amorphous silicon layer 57, and a passivation layer 56 are sequentially formed over the substrate 1. When the drain contact hole (reference 32 of Figures 2 and 3D) is patterned through the passivation layer 56, a gate pad contact hole 44 is formed through the gate insulating layer 50, the amorphous silicon layer 57, and the passivation layer 56. Therefore, a portion of the gate pad 21 is exposed by the gate pad contact hole 44. When a gate pad electrode 34 is formed over the gate pad 21, they are electrically connected to each other via the data pad contact hole 42.